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NXP, B.V.
NXP INTELLECTUAL PROPERTY & LICENSING
M/S41-SJ
1109 MCKAY DRIVE
SAN JOSE, CA 95131

EXAMINER	
WRIGHT, BRYAN F	

ART UNIT	PAPER NUMBER
2431	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/535,755	SCHROEDER ET AL.	
	Examiner	Art Unit	
	BRYAN WRIGHT	2431	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 April 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

FINAL ACTION

1. This action is in response to amendment filed 3/31/2010. Claims 1-14 are pending.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

2. Claims 1-14 are rejected under 35 U.S.C. 101 because the claimed invention lacks patentable utility. The Examiner contends applicant's claimed invention is directed towards controlling program logic on a microcontroller, specifically, executing programmatic behavior step. Once the execution of the programmatic behavior step occurs, no tangible output is produce. The Examiner respectfully submits transitioning thru programmatic behavior steps without producing a tangible result lacks utility. While the cited prior art teaches the same capability, each art is directed towards a utility.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 12 and 13 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Examiner contends applicant's claim limitation element as amended, "wherein the one of the different instruction sequences is located at the program address" lacks support within the original disclosure.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cohen (EP 0690370 A2) in view of Anderson et al. (US Patent Publication No. 2003/0084336 and Anderson hereinafter).

5. As to claim 1, Cohen teaches a microcontroller the programming of which is carried out in at least one machine-dependent assembler language in which the assembler commands, with the exception of conditional program jumps or program branches (i.e., robust jump [pg. 9, 10- 25]), respectively, can be executed independently of data, comprising at least one random number generator (i.e., pseudo random generator [Cohen, claim 10]) assigned to the microcontroller can be executed (Cohen, claim 10), by means of which the program jumps and program branches (i.e., robust jump [Cohen, claim 9]) are executed in dependence on the state of the random number generator and independently of the internal state of the programming of the microcontroller value prior to ending the instruction (i.e., ... teaches condition bit and Request Jump parameter to robust jump program [pg. 9, 10-25] such that both parameter are derived by a pseudo random generator signal [Cohen, claim 10]).

Cohen does not expressly teach the use of a Random Number Generator (RNG) for purposes of microcontroller activity (e.g., controlling a Jump Condition). However, the feature using a random number generator to control microcontroller activity was ready available and was well known in the art at the time of applicant's original filings and would have been an obvious modification of the system disclosed by Cohen as

introduced by Anderson. Anderson discloses the use of a RNG for control of microcontroller activity (e.g., controlling a Jump Condition with in the microcontroller) (to provide microcontroller architecture such that the internal activities of the microcontroller are controlled by a RNG [par. 23]).

Therefore, given Anderson's ability to control microcontroller activity using programmatic behavior steps, a person having ordinary skill in the art at the time of the invention would have recognized the desirability and advantage of modifying Cohen to enhance the security and speed of performing the steps thereby enhancing the microcontroller's activity by employing the well known feature of a microcontroller utilizing random number generation means to control behavior steps disclosed above by Anderson.

6. As to claim 2, Cohen teaches a microcontroller, characterized by at least one, in particular bit-addressable (i.e., a 8-bit addressable register [fig. 6]), random number register (i.e., load clock division register) assigned to the random number generator (i.e., .. teaches a pseudo random number generator [Cohen, claim 10] controlled by a clock division register [430, fig. 4]).

7. As to claim 3, Cohen teaches a microcontroller, characterized by an embodiment as a smartcard controller smartcard controller including the microcontroller of claim 1 (i.e., ... teaches a smart card is inherently a microprocessor [pg. 4, lines 40-45]).

8. As to claim 4, Cohen teaches a electrical or electronic device controlled by means of at least one microcontroller (i.e., teaches a microcode controller [pg. 5, lines 20-25]).

9. As to claim 5, Cohen teaches a method for processing the programming of a microcontroller executed in at least one machine-dependent assembler language, the assembler commands, with the exception of conditional program jumps or branches (i.e., teaches a robust jump conditional program [pg. 9, lines 10-25]), being executed essentially independently of data, characterized in that the program jumps or program branches (i.e., robust jump [Cohen, claim 9]) are executed in dependence on the state of at least one random number generator and/or independently of the internal state of the programming of the microcontroller (i.e., ...teaches a random generator operable to generate a signal to execute instruction [Cohen, claim 10] ... further teaches control algorithm [pg. 12, lines 5-50]).

Cohen does not expressly teach the use of a Random Number Generator (RNG) for purposes of microcontroller activity (e.g., controlling a Jump Condition). However, the feature using a random number generator to control microcontroller activity was ready available and was well known in the art at the time of applicant's original filings and would have been an obvious modification of the system disclosed by Cohen as introduced by Anderson. Anderson discloses the use of a RNG for control of microcontroller activity (e.g., controlling a Jump Condition with in the microcontroller) (to

provide microcontroller architecture such that the internal activities of the microcontroller are controlled by a RNG [par. 23]).

Therefore, given Anderson's ability to control microcontroller activity using programmatic behavior steps, a person having ordinary skill in the art at the time of the invention would have recognized the desirability and advantage of modifying Cohen to enhance the security and speed of performing the steps thereby enhancing the microcontroller's activity by employing the well known feature of a microcontroller utilizing random number generation means to control behavior steps disclosed above by Anderson.

10. As to claim 6, Cohen teaches a method, characterized in that the random number generated by the random number generator read via software via registers (i.e., clock division register) and the random number read is then evaluated with a conditional program jump or branch (i.e., ... teaches a requested jump 3arameter read into robust jump program [pg. 9, lines 10-15]).

11. As to claim 7, Cohen teaches a method, characterized in that, if at least one, in particular bit-addressable (i.e., 8 bit-address register [300, fig. 5]), random number register (i.e., clock division register) is present, testing per bit of the random number register and a conditional jump or branch is carried out (i.e., ... teaches logic for carrying out the conditional jump [pg. 9, 10- 25]).

12. As to claim 8, Cohen teaches a method, characterized by the implementation of at least one assembler command ("branch on random bit"), a defined bit of the random number register (i.e., clock division register) being supplied, in particular directly, to a condition input for the conditional jump or branch [pg. 9, lines 10-25].

13. As to claim 9, Cohen teaches a method, characterized in that at least one Arithmetic Logic Unit (ALU) flag controlling the conditional jumps or branches is replaced (i.e., instruction decoder), in particular via the software, by at least one bit of the random number register (i.e., clock division register), so that the conditional jumps or branches corresponding to the bit of the Arithmetic Logic Unit are controlled by the bit of the Random Number Register (i.e., ...teaches a instruction decoder providing input to perform the robust jump [460, fig. 7] ... further teaches Condition Bits parameter for control logic of the conditional jump [pg. 9, 10-15]).

14. As to claim 10, Cohen teaches a use of a microcontroller for completely concealing the programming running on the microcontroller, so that at least one program running on the microcontroller is unpredictable and non-reproducible for an external observer (i.e., ... teaches a execution unit containing programming logic [74, fig. 4]).

15. As to claim 11, Cohen teaches microcontroller comprising: a central processing unit; a memory accessible to the central processing unit, wherein the memory

comprises instructions and wherein the central processing unit is configured for: accessing the instructions, wherein the instructions comprise different instruction sequences for accomplishing a same desired action and where each instruction sequence produces a same result value for a same input value (i.e., ... teaches a sequence of computer instruction [pg. 10- 14]); receiving a random number associated with an instruction sequences (i.e., ...teaches pseudo-random generator generating a signal to control instruction [Cohen, claim 10]; receiving the same input value (i.e., ... teaches receiving duplicate input signals [10, fig. 2]); and executing the one of the different instruction sequences associated with the random number using the same input value to produce the same result (i.e., ...teaches executing the instruction base on a signal from a pseudo random generator [claim 10]. Cohen does not expressly teach the use of a Random Number Generator (RNG) for purposes of microcontroller activity (e.g., controlling a Jump Condition). However, these features are well known in the art and would have been an obvious modification of the system disclosed by Cohen as introduced by Anderson. Anderson discloses the use of a RNG for control of microcontroller activity (e.g., controlling a Jump Condition with in the microcontroller) (to provide microcontroller architecture such that the internal activities of the microcontroller are controlled by a RNG [par. 23]). Therefore, given Anderson's ability to control microcontroller activity using programmatic behavior steps, a person having ordinary skill in the art at the time of the invention would have recognized the desirability and advantage of modifying Cohen to enhance the security and speed of performing the steps thereby enhancing the microcontroller's activity by employing the well known

feature of a microcontroller utilizing random number generation means to control behavior steps disclosed above by Anderson.

16. As to claim 12, Cohen teaches microcontroller where the instructions further comprise a jump instruction (i.e., robust jump [pg. 9]) subject to a condition which if true directs the central processing unit to a program address (i.e., ... teaches jump instruction to machine locations [Cohen, claim 9]), where the one of the different instruction sequences is located at the program address (i.e., ...teaches location, and wherein the random number is associated with the instruction sequence via the program address [Cohen, claims 9]).

17. As to claim 13, Cohen teaches microcontroller where the instructions further comprise a jump instruction (i.e., robust jump [pg. 9]) subject to a condition which if true directs the central processing unit to a program address (i.e., ... teaches jump instruction to machine locations [Cohen, claim 9]), wherein the one of the different instruction sequences is located at the program address (i.e., ... teaches mapping scheme for controlling microcontroller activities [abstract]), and wherein the random number is associated with the one of the different instruction sequences via the condition (i.e., ... teaches a pseudo random generator operable to generated a signal to control instruction [claim 10]).

18. As to claim 14, Cohen teaches microcontroller where the random number (i.e., random number signal [Cohen, claim 10]) is generated by a random number generator (i.e., teaches a pseudo random generator) assigned to the microcontroller [Cohen, claim 10].

Response to Arguments

Examiner Response - Claim Rejections under 35 U.S.C. 101

With regards to applicant's remarks of:

> **" ... Office Action contends that the claimed invention is directed towards controlling program logic on a microcontroller, specifically, executing programmatic behavior steps. The Office Action also asserts that once the execution of the programmatic behavior step occurs, no tangible output is produced. The Office Action further submits transitioning thru programmatic behavior steps without producing a tangible result lacks utility. However, Applicants respectfully submit that there is no basis for the stated rejection. There is no requirement that the claimed invention must produce some kind of tangible output. Section 101 states: Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title. Furthermore, the MPEP states: If at any time during the examination, it becomes readily apparent that the claimed invention has a well-established utility, do not impose a rejection based on lack of utility. An invention has a well-established utility if (i) a person of ordinary skill in the art would immediately appreciate why the invention is useful based on the characteristics of the invention (e.g., properties or applications of a product or process), and (ii) the utility is specific, substantial, and credible. Applicants assert that the claimed invention qualifies under both requirements i) and ii) of the MPEP. Additionally, per the language of Section 101, Applicants assert that the claimed invention is directed towards patentable utility. Specifically, Applicants direct attention to the Specification of the instant application; therein can be found several examples of the utility of embodiments of the claimed invention. One example of the utility of an embodiment of the claimed invention is described in page 3, lines 3-14 of the specification. This portion describes utility of an embodiment of the claimed invention in increasing the difficulty in making conclusions regarding the process or data in the current action of a microcontroller from the perspective of an outside observer or**

> **attacker. Thus, for example, the security of a system may be increased by an embodiment of the claimed invention. Therefore, Applicants respectfully submit claims 1-14 satisfy the requirements set forth in the MPEP with respect to determining whether a claimed invention complies with 35 U.S.C. 101.**

The Examiner respectfully submits that applicant's claim 1 is directed towards programming steps. Accordingly, the program steps do not produce a useful and tangible result as required under 35 U.S.C. 101. Applicant's claim 1 reads:

> 1.**(previously presented) A microcontroller the programming of which is carried out in at least one machine-dependent assembler language in which the assembler commands, with the exception of conditional program jumps or program branches, respectively, are executed independently of data, comprising at least one random number generator assigned to the microcontroller, by means of which the program jumps and program branches are executed in dependence on the state of the random number generator and independently of the internal state of the programming of the microcontroller.**

The described occurrence of a conditional program jump under random means is not a useful and tangible result as necessitated by 35 U.S.C. 101. Therefore the Examiner maintains the rejection for claims 1-14 under 35 U.S.C. 101.

Examiner Response –

Claim Rejections under 35 U.S.C. 112, first paragraph

Applicant states:

> "**Applicants provided two individual citations to point out and describe support for the claimed language of "program address" within the specification. For at least this reason, Applicants respectfully request reconsideration of the response below in its entirety. In the previous response, Applicants respectfully submitted that the limitation related to one of the different instruction sequences located at the program address is supported by the specification, even though there may not be explicit antecedent basis for the language. This language is supported by the**

specification, for example, at least on page 3, lines 3-14, which states "the desired action can be selected from a large number of possible instruction sequences by the use of a Random Number Generator" (emphasis added) and "By means of a random program run of this kind." While the above section of page 3, lines 3-14, does not explicitly refer to the different instruction sequences located at the program address, the description at page 1, lines 14-29, describes how different instructions are associated with memory locations or program addresses. In response to the current rejection, Applicants maintain the previous response and even though the reasoning in the Office Action, mailed 01/04/2010, reasserts that the "cited specification does not mention the limitation element 'program address' "(page 12, Response to Arguments), Applicants again assert that the description at page 1, lines 14-29, explicitly describes the use of program addresses or values. The cited language is clear and descriptive, and it appears that the response included in the Office Action is based solely on the first above-cited portion of the specification. However, both of the cited portions support the indicated claim language. Therefore, Applicants respectfully submit that the detailed description of the specification provides support for each of these claim limitations because embodiments of the process are described to realize jumps or branches based on conditions to determine how the instructions at each location or program address proceed. While the specification may not explicitly provide antecedent basis for the exact language used in the claims, Applicants respectfully submit that the indicated language finds considerable support in the specification, including the support described above. See, MPEP 608.01(o) ("an applicant is not limited to the nomenclature used in the application as filed"). Furthermore, 37 C.F.R. 1.75(d)(1) requires the terms and phrases used in the claims must find clear support or antecedent basis in the description so that the meaning of the terms in the claims may be ascertainable. In other words, support is required, and antecedent basis is simply one way of providing support, but is not the only way to provide support for the limitations of the claim. Here, although the language of the claims differs somewhat from the actual nomenclature provided in the specification, Applicants respectfully submit that the claim language is nevertheless supported by the specification because the claims recite limitations that are well within the scope of the embodiments described in the specification. Moreover, although the MPEP indicates that the use of a variety of terms can be confusing, Applicants respectfully submit that the terms used in the claims do not cause such confusion. On the contrary, the language of the claims is ascertainable from the specification, as shown by the explanation provided above. Therefore, Applicants assert the claims are supported by the specification as filed because the language is within the scope of the written description provided in the specification, and the language does not cause confusion as to the meaning of the claims.

> **Accordingly, Applicants respectfully request that the rejections of claims 12 and 13 under 35 U.S.C. 112, first paragraph, be withdrawn.**

The Examiner notes applicant's statement of, "**While the above section of page 3, lines 3-14, does not explicitly refer to the different instruction sequences located at the program address".** The Examiner respectfully submits that this statement acknowledges the fact that applicant's specification lacks explicit support for the claim limitation of "**wherein the one of the different instruction sequences is located at the program address**". Therefore the Examiner maintains the rejection made under 35 U.S.C. 112, first paragraph for claim 12 and 13.

Examiner Response –

Claim Rejections under 35 U.S.C. 103(a)

Applicant argues:

> "**Independent Claim 1 Claim 1 is patentable over the combination of Cohen and Anderson because the rejection of claim 1 is improper. The rejection of claim 1 is improper because 1) the Office Action does not establish a prima facie rejection for claim 1, and 2) the proposed combination of Cohen and Anderson is improper because the proposed combination would render Cohen unsatisfactory for its intended purpose. Applicants respectfully reaffirm Applicants' assertions made in response to the previous Office Action, mailed 5/29/2009, and re-state the arguments with further elaboration, explanation, and evidence to support the specific reasoning. In particular, Applicants assert that the reasoning presented below shows that there is substantial evidence against the suggested combination of references asserted by the Office Action. For example, Applicants submit that the suggested combination is improper because the combination suffers from a lack of rational underpinning and is improper. Specifically, the proposed combination is improper because the articulated reasoning is not supported by the references.**

The Examiner contends the example given by Applicant of "**Applicants submit that the suggested combination is improper because the combination suffers from a lack of rational underpinning and is improper",** cannot be construed to have possess merit in view of the teaching of both Cohen and Anderson.

With regards to applicant's secondary remarks as to why the rejection is improper of:

> "**Also, the device of Cohen to provide an alert to an outside system, provide selective timing compatibility, and generate state signals for the process of the microcontroller would be insufficient for at least these intended purposes**".

The Examiner contends Anderson's microprocessor can jump to a sequence of instruction under random means. See Anderson paragraph 23. The Examiner respectfully submits Anderson's microprocessor is an enhancement over the Cohen's microprocessor. Additionally, the Examiner contends that the applicant is mistaken to state that Anderson's microprocessor can not be instructed (e.g., generated specific signals) in the same manner as Cohen's original microprocessor.

With regards to applicant statement of:

> **"The analysis must be made explicit. Id. Additionally, rejections based on obviousness cannot be sustained by mere conclusory statements; instead there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness. Here, the Office Action fails to provide an explicit reason as to why the limitations of claim 1 would have been obvious. In particular, the Office Action simply states: Cohen does not expressly teach the use of a Random Number Generator (RNG) for purposes of microcontroller activity (e.g., controlling a Jump Condition). However, the feature using a random number generator to control microcontroller activity was ready available and was well known in the art**

at the time of applicant's original filings and would have been an obvious modification of the system disclosed by Cohen as introduced by Anderson. Anderson discloses the use of a RNG for control of microcontroller activity (e.g., controlling a Jump Condition with in the microcontroller) (to provide microcontroller architecture such that the internal activities of the microcontroller are controlled by a RNG [par. 23]): Therefore, given Anderson's ability to control microcontroller activity using programmatic behavior steps, a person having ordinary skill in the art at the time of the invention would have recognized the desirability and advantage of modifying Cohen to enhance the security and speed of performing the steps thereby enhancing the microcontroller's activity by employing the well known feature of a microcontroller utilizing random number generation means to control its activity disclosed above by Anderson. The Office Action is merely conclusory in stating that the proposed modification of Cohen would "enhance the security and speed of performing the steps." Applicants submit that the Office Action offers no explicit analysis to support the assertion that the proposed modification would afford such an improvement. Additionally, there is no analysis as to how the proposed modifications would be implemented into the system of Cohen because the system of Cohen teaches a security aspect which reacts upon detection or tampering. Therefore, it is not obvious how the proposed modification would "enhance the security" of the system. Additionally, there is no analysis to show how the proposed modification might enhance the speed of the system taught by Cohen because there does not appear to be an advantage in the proposed combination over the system of Cohen relating to processing speed or reduction in the number of processes. Therefore, Applicants submit that there is no showing or explanation of how it would be obvious to combine the cited references, or that the indicated limitation might otherwise be obvious in light of the cited references".

The Examiner contends combining Anderson's processor instruction jump capability will allow for performance enhance of Cohen present microprocessor. Additionally, the Examiner contends that the sequence instruction jumps are random and that such random behavior can not easily trace by potential attackers thereby inherently increasing security.

With regards to applicant's remarks of:

"Moreover, in addition to the lack of showing and analysis in support of the proposed combination, Applicants submit that there is substantial evidence against the suggested combinations for reasons further described below. Therefore, the Office Action fails to establish aprimafacie rejection for claim 1 because the Office Action does not provide articulated reasoning with some rational underpinning in the rejection of claim 1. Accordingly, Applicants respectfully submit that the rejection of claim 1 under 35 U.S.C. 103(a) should be withdrawn because the Office Action fails to establish aprimafacie rejection. The Proposed Combination is Improper Furthermore, even if the combination of Cohen and Anderson were to teach all of the limitations of the claim, the proposed combination of Cohen and Anderson nevertheless improper. In asserting a combination of references as a basis for an obviousness rejection, the proposed combination or modification cannot change the principle of operation of the prior art. MPEP 2143.01 (VI). In addition, the combination of references cannot render the prior art unsatisfactory for its intended purpose. MPEP 2143.01 (V). Here, the combination of teachings proposed in the Office Action would change the principle of operation of Cohen and would render the device of Cohen unsatisfactory for its intended purpose. The proposed combination of Cohen and Anderson is improper because the use of a random number generator, as taught by Anderson, within the device of Cohen would render the device of Cohen unsatisfactory for its intended purpose. Anderson generates pseudo-random bits with a free-running pseudo-random number generator based on a shift register. The bit stream generated by the pseudo-random number generator is sampled upon execution of a set-random-carry command. Anderson, paragraph 23. In contrast, Cohen teaches that the performance of a conditional robust jump is dependent upon the contents and integrity of the composite condition signal within a single machine cycle. Cohen, page 8, line 43 to page 9, line 4; Fig. 7. In other words, the jump is decided based on conditions within the microcontroller. The jump is determined by the integrity of the data which allows a GoError signal to be activated. Nevertheless, despite the teaching of Cohen that the jump is dependent on the data integrity, the Office Action proposes to modify the teaching of Cohen to use a random number generator bit stream to trigger the jump, instead of a data integrity check. This proposition to use a random number generator not only removes the use of the code taught by Cohen (Cohen, page 9, lines 10-25) to perform a jump based on data integrity, but further would appear to eliminate the ability for the teachings of Cohen to generate the GoError signal because this modification would, in turn, prevent the system from informing the outside world of a data integrity problem, as taught by Cohen. Moreover, the teachings of Cohen are directed towards a tamper-resistant system which employs the use of a security comparator and a security sensor array to detect an "expected state" within the device of

Cohen. Cohen, page 7, lines 23-51. These components execute various lines of code taught by Cohen in order to adapt to and prevent compromise due to tampering. This is different from the system of Anderson which employs a number generator. If the proposed modification of Cohen were implemented as suggested by the Office Action the combination would render the entire security and signal sensitive "conditional jump" of Cohen unsatisfactory for its intended purpose. Nevertheless, without support or offering of evidence, the Office Action asserts: "...it would have been obvious to those skilled in the art to perform the modification in order to enhance the performance and security of Cohen's microcontroller activity." Office Action (01/04/2010, page 12, Response to Arguments, 103 Remarks) Applicants assert that the reasoning provided in the Office Action does not find support in the teachings of either Cohen or Anderson because there is no support for the assertions of "enhanced performance and security." Furthermore, the Office Action does not address or recognize the timing sensitive aspect of the device of Cohen. Specifically, Cohen teaches a balance of speed and optimization which allows the processor to be selectibly timing compatible with an existing processor. Cohen, page 2, lines 23-30. It appears that the random nature of the proposed combination would not facilitate this aspect of the invention and would further render the device of Cohen unsatisfactory for its intended purpose. Moreover, even if it were possible to implement the teaching of Anderson without replacing the aforementioned teachings of Cohen, the proposed modification of Cohen would also make it difficult or impossible to prevent conflicting signals from occurring with respect to controlling and tracking the jump signals because the jump criteria for Cohen and Anderson are dissimilar. Furthermore, there is no explanation of how the random number generator approach of Anderson might be implemented into the teachings of Cohen without rendering Cohen unsatisfactory for, first, communicating an error signal upon detection of a data integrity compromise and preventing a jump or branch in the microcontroller and, second, associating the jump with a signal received from an instruction decoder because Anderson teaches use of a random number generator to control jumps and branches in the program of the microcontroller. Therefore, combining the references of Cohen and Anderson, as proposed in the Office Action, would render the device of Cohen unsatisfactory for its intended purpose because use of the bit sampling of the bit stream generated by the random number generator described in Anderson would prevent the system of Cohen from performing a jump based on data integrity, from demonstrating selectable timing compatibility with an existing processor, and, further, would appear to prevent Cohen from generating the GoError signal which would further prevent the device of Cohen from informing the outside world of a data integrity problem. Accordingly, Applicants respectfully assert independent claim 1 is

> **patentable over the cited references because the proposed combination of references is improper. Independent Claims 5 and 11 Applicants respectfully assert independent claims 5 and 11 are patentable over the proposed combinations of Cohen and Anderson at least for similar reasons to those stated above in regard to the rejection of independent claim 1. Each of claims 5 and 11 recites subject matter which is similar to the subject matter of claim 1 discussed above. Although the language of these claims differs from the language of claim 1, and the scope of these claims should be interpreted independently of other claims, Applicants respectfully assert that the remarks provided above in regard to the rejection of claim 1 also apply to the rejection of these claims".**

The Examiner contends that the "unsatisfactory" basis for which the applicant renders Cohen and Anderson to be incompatible to combine cannot be sufficiently equated. Anderson discloses that his microprocessor has an additional instruction that can support the processor ability to jump between instruction sequences by random means. The microprocessor of Anderson is still able to function as a microprocessor and therefore can be instructed in the matter to produce the desired behavior as Cohens'. The Examiner contends that the jump capability is an enhancement over Cohen's conventional microprocessor. With regards to applicant's remarks of "...would appear to prevent Cohen from generating the GoError signal which would further prevent the device of Cohen from informing the outside world of a data integrity problem", the Examiner respectfully disagrees. There is nothing that would suggest that is signal cannot be asserted. Hardware wise the I/O of Anderson's microprocessor can support this signal. Again, the Examiner contends Anderson's microprocessor can be programmed the exact same way to accomplish the exact results as Cohen, however Anderson's microprocessor has the added benefit of the additional instruction that can

support the processor's ability to jump between instruction sequences using random means.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to BRYAN WRIGHT whose telephone number is (571)270-3826. The examiner can normally be reached on 8:30 am - 5:30 pm Monday -Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William Korzuch can be reached on (571) 272-7589. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/BRYAN WRIGHT/
Examiner, Art Unit 2431
/Syed Zia/
Primary Examiner, Art Unit 2431